IN THE CLAIMS

Claims 1-17 (Canceled).

18. (Currently Amended) A semiconductor integrated circuit device, comprising:

a logic circuit including a logic transistor formed of an insulted gate type field effect transistor as a component thereof and executing a prescribed processing; and

memory circuitry for storing at least data to be used by said logic circuit, said memory circuitry including a first circuit configured for receiving first and second voltages a difference of which provides ~~a first voltage of~~ a first amplitude and a second circuit configured for receiving third and fourth voltages a difference of which provides ~~a second voltage of~~ a second amplitude, the second amplitude being greater than the first amplitude,

said first circuit including as a component thereof a first-type insulated gate field effect transistor having a ~~single~~ first gate insulting film of a single-gate structure different from a stacked gate structure having two electrodes stacked with an insulating film placed in between ~~same at least in thickness as said logic transistor~~, said second circuit including as a component thereof a second-type insulated gate field effect transistor having a ~~single~~ second gate insulating film of the single-gate structure, the second gate insulating film being thicker than [[a]] the first gate insulating film, [[of]] said logic transistor having a gate insulating film with a thickness of the first gate insulating film.

19. (Previously Presented) The semiconductor integrated circuit device according to claim 18, wherein

said memory circuitry further includes:

a memory cell array having a plurality of memory cells arranged in rows and columns, the memory cell including said second-type insulated gate field effect transistor as a component thereof.

20. (Previously Presented) The semiconductor integrated circuit device according to claim 19, wherein

said memory circuitry further includes:

a plurality of sense amplifier circuits provided corresponding to the columns of the memory cells, each for sensing and amplifying data of a memory cell on a corresponding column,

the sense amplifier circuit including said first-type insulated gate field effect transistor as a component thereof.

21. (New) The semiconductor integrated circuit device according to claim 20, wherein

said memory circuitry further includes:

a sense power supply line; and

a plurality of sense drive transistors each provided for a predetermined number of the sense amplifier circuits and being formed of the second-type insulated gate field effect transistor, for coupling, when made conductive, corresponding sense amplifier circuits to said sense power supply line.

22. (New) The semiconductor integrated device according to claim 20, wherein

said memory circuit further includes:

a sense power supply line; and

a plurality of sense amplifier drive transistors each provided for a predetermined number of the sense amplifier circuits and being formed of the first-type insulated gate transistor, for coupling the sense power supply line to the sense amplifier circuits, back gates of said plurality of sense amplifier drive transistors receiving a voltage larger in absolute value than a voltage on said sense power supply line.

23. (New) The semiconductor integrated circuit device according to claim 22, wherein:

said memory cell array is divided into a plurality of memory blocks along directions of the rows and columns; and

the sense amplifier drive transistor is provided in a region between memory blocks adjacent in the directions of the rows.

24. (New) The semiconductor integrated circuit device according to claim 21, wherein:

said memory cell array is divided into a plurality of memory blocks along directions of the rows and the columns;

the sense amplifier circuit is provided in a region between memory blocks adjacent in the direction of the columns; and

the sense amplifier drive transistor is provided in a crossing region of a region for arranging the sense amplifier circuit and a region between memory blocks adjacent in the direction of the rows.